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Design of Flip-Flops for High Performance VLSI Applications Using Different CMOS Technology's

Shillu Elsa Thomas
shilluelsathomas@gmail.com
Musaliar College of Engineering and Technology
Pathanamthitta, Kerala

ABSTRACT

In this paper low power, high speed design of SET, DET, TSPC and C2CMOS Flip-Flop are designed and analysed. As these flip flop have a small area and low power consumption they can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The Flip-Flops are analyzed at 90nm technologies. The above designed Flip-Flops and Latches are compared in terms of its transistor count, power dissipation and propagation delay using DSCH and Microwind tools. This project proposes low power high speed design of flip flops in which True Single Phase Clocking (TSPC) and C2CMOS flip flop compared with existing flip flop topologies in term of its transistor count, power dissipation, propagation delay, parasitic values with the simulation results in microwind.

Keywords: ***2 stage OP-AMP, CMOS, Gain, Phase Margin, and Unity Gain Band Width.***

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1. INTRODUCTION

For high performance VLSI chip-design, the choice of the back-end methodology has a significant impact on the design time and the design cost. Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore various following flip flop topologies were designed for some dedicated applications.

Flip-Flop is a circuit that stores a logical state of one or more data input signals in response to a clock pulse. For CMOS technology topology selection, power dissipation and speed are very important aspect especially for designing Clocked Storage Element (CSE) for high-speed and low-energy design like portable batteries and microprocessors. Various classes of flip-flops have been projected to achieve high-speed and low-energy operation. A flip-flop is a bistable circuit which stores a logic state of 0 or 1 in response to a clock pulse with one or more data inputs. Design of some flip flop architectures and analyses it in term of power consumptions and propagation delay.

Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. Following are most high performance flip flops.

[1] Single Edge-Triggered Flip-Flop (SET)
[2] Double Edge-Triggered Flip-Flop (DET)
[3] True Single-Phase-Clock Flip-Flop (TSPC)
[4] Clocked CMOS Flip-Flop (C2CMOS)

At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops otherwise it is called as single edge triggered Flip-Flops.

1.1SINGLE EDGE TRIGGERED FLIP-FLOP

The efficient architecture of Single Edge Trigger flip flop which is based on negative edge trigger given in following figure1. In that when the *clock* is high; the master latch is updated to a new value of the input *D*. The slave latch produces the previous value of *D* on the output *Q*. When the *clock* goes down, the master latch turns to memory state. The slave circuit is updated. The change of the clock from 1 to 0 is the active edge of the clock. This type of latch is a negative edge flip flop.

The reset function is added by a direct grounding the input signal present at feedback path of the master and slave memories, using nMOS devices. This added circuit is equivalent to an asynchronous Reset, which means that *Q* will be reset to 0 when *Reset* is set to 1, without waiting for an active edge of the clock. The above structure is drawn with the help of DSCH tool represented into cmos and passes transistor logic

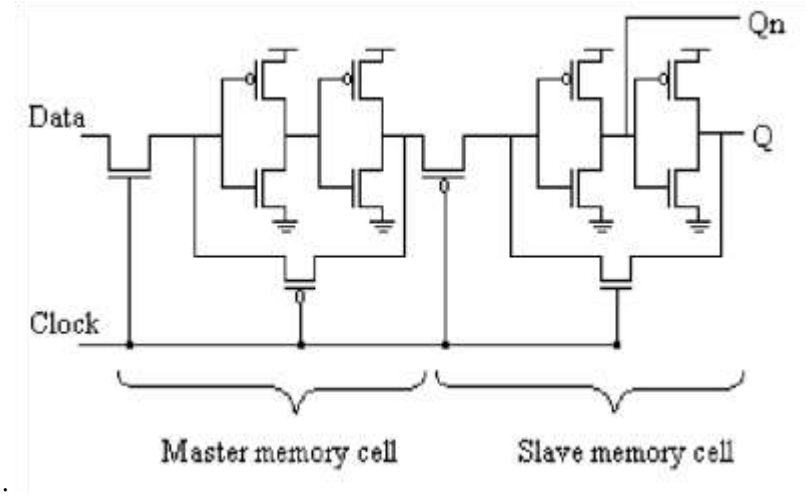

Figure 1: Efficient Architecture of SET D Flip Flop

1.2 DOUBLE EDGE TRIGGERED FLIP FLOP

At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops otherwise it is called as single edge triggered Flip-Flop

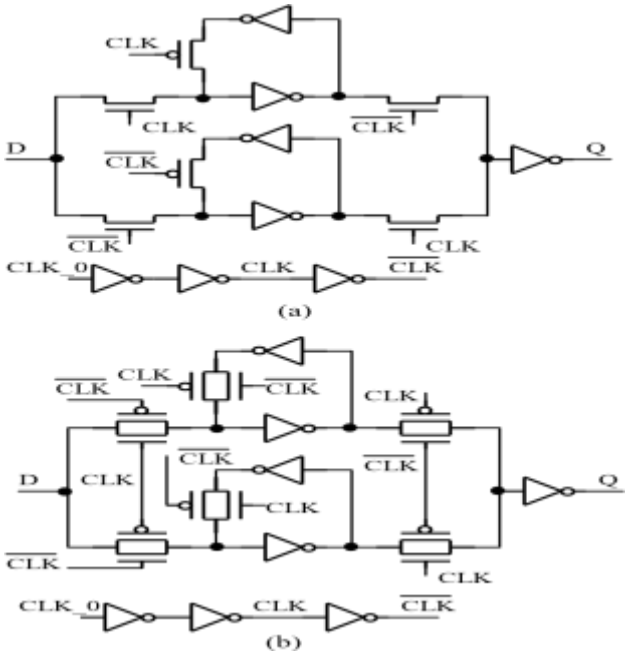

Figure 2. (a)The Design of CMOS DET flip-flop (b) A Modified design of cmos DET flip-flop

1.3 TRUE SINGLE PHASE CLOCK

8 Transistor T flip-flop and 6 transistors latch Circuit 8 during recurring clock intervals to transistors flip-flop the pioneer CMOS traditional flip-flop circuit is reported in positive edge triggered 5 Transistor D latch. When CLK and input IN are high then the transistors M1, M5 is OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the values of input, it becomes output. It also acts as
a flip-flop when the input IN has less pulse width.

From simulation results, it is concluded that TSPC Flip-Flop is having less power consumption. This is because it is having only 5 transistors, only one transistor being clocked and that clock is having short pulse train. By applying MTCMOS leakage power minimization technique, the leakage power is minimized when technology scales down.

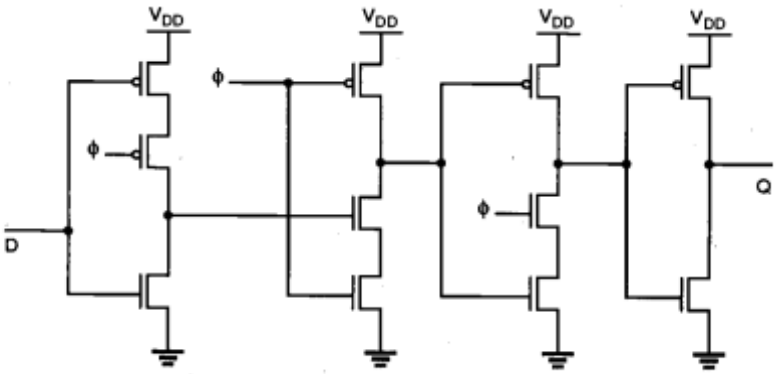

Figure 3: Negative edge trigger TSPC flip flop

1.4 CLOCKED CMOS

Clocked CMOS circuits with gradually rising and falling power-clock are expected to obtain a significant energy saving When clock is low, for the master stage it enters into the evaluation mode ie, the transistor M3 and M4 will be in the ON condition and the circuit acts like an inverter circuit so when d=0 the x will be equal to 1 and vice versa .For the slave stage it enter in the hold mode ie, both the transistors M7 andM8 will be in the previous state

When the clock is high, here the master stage enter into the hold state ie, both the transistor M4 and M3 are in the OFF condition ie, the output x will remain in the previous state. Now the slave stage enter into the evaluation state ie, both the transistors M7 andM8 will be in the ON condition and the final output Q will be in the inverter state of the input signal given ie when x=1 Q will be equal to 0 and vice versa or I other words the final output obtained will be same as the final.

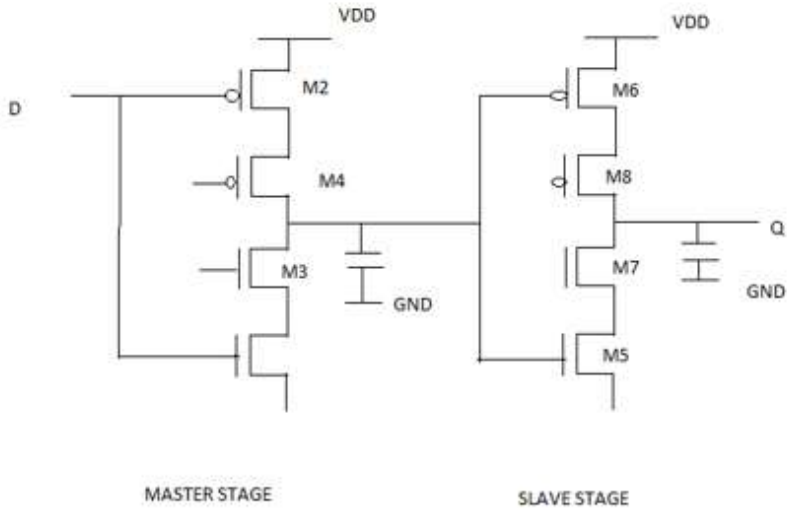

Figure 8: Clocked CMOS

2. RESULTS AND DISCUSSIONS

3.1 Layout Diagram

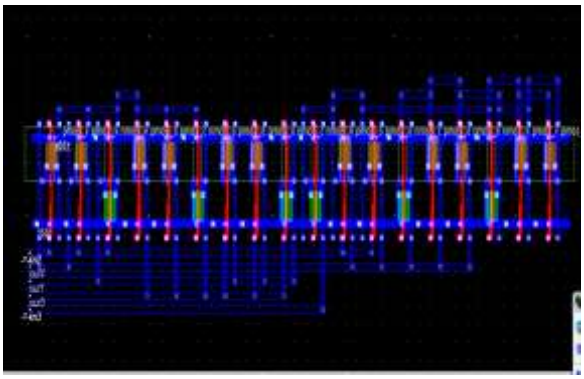

Figure 9: SET

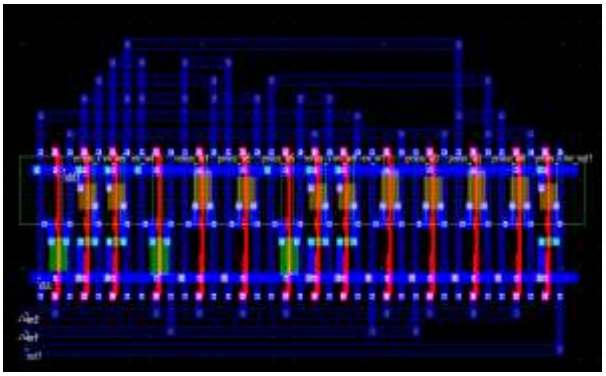

Figure 10: DET

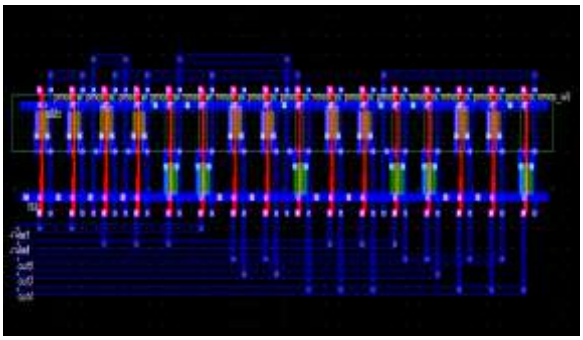

Figure 11: TSPC

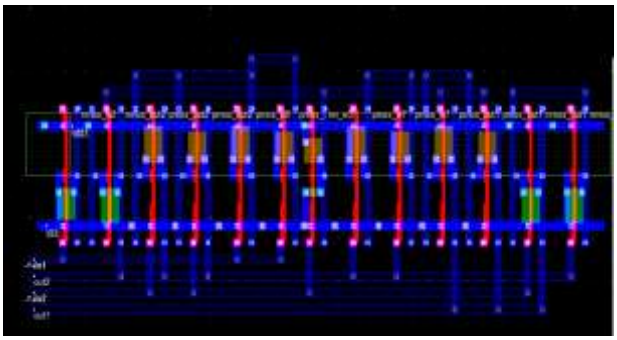

Figure 12: C2MOS

3.2 VOLTAGE V/S TIME GRAPH

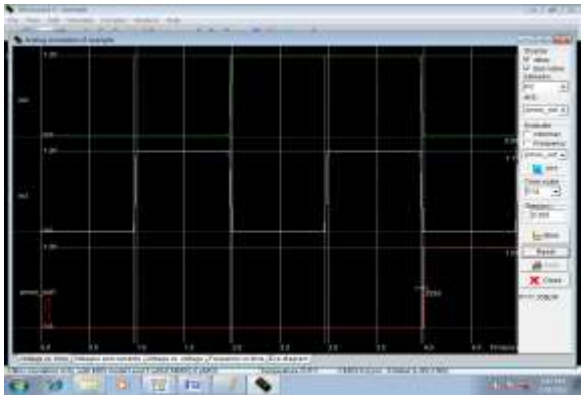

Figure 13: SET

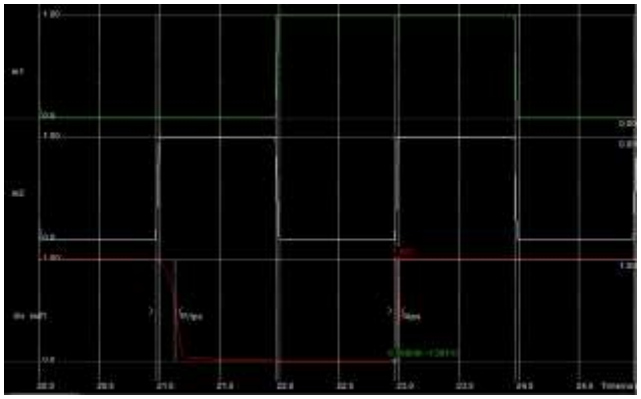

Figure 14: DET

PROPAGATION DELAY=28ps

POWER DISSIPATION=13.521µW

PROPAGATION DELAY=15ps

POWER DISSIPATION=11.38µW

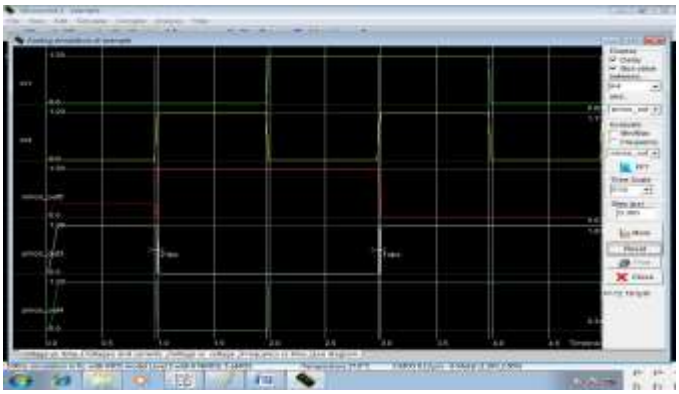

Figure13: TSPC

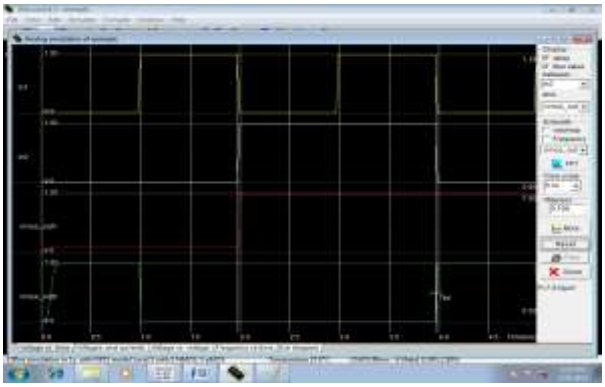

Figure 14: C2MOS

PROPAGATION DELAY =14ps

POWER DISSIPATION=7.512µW

PROPAGATION DELAY=7ps

POWER DISSIPATION=12.161µW

3. CONCLUSION

In this paper, an exhaustive analysis and design methodology for commonly used high-speed flip-flops topologies in 90nm CMOS technologies have been carried out. The comparison has been performed with the area, delay, and power dissipation. The impact of layout parasitic has been included in the transistor-level design phase. The flip-flops chose for a thorough comparative analysis, whose results are reported in section II and III. According to the presented results, the fastest topology is the C2CMOS and DET since the delay, with respect to area and number of transistor count TSPC and C2CMOS are better while with respect to power dissipation SET shows a better result, the best low-power flip-flops are the SET. Moreover, the best topology under clock skew and less propagation delay are DET and C2CMOS.

We conclude that efficient design architecture based on power dissipation, propagation delay and transistor counts for portable applications are TSPC, SET, DET and C2CMOS Flip-flop. Considerate the suitability of flip-flops and selecting the best topology for a given application is an important issue; the low power design SET is suitable for portable applications.

Architecture	SET	DET	TSPC	C2MOS
Technology	CMOS 90nm, 6 Metal Copper- strained SiGe Lowk (1.2V-2.5V).			
Voltage rating	1.20V			
Power Dissipation (µW)	11.338µW	13.521µW	12.161µW	7.512µW
Propagation Delay (ps)	22pF	15pF	14pF	7pF
Transistor count	14	16	10	12

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