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Hybrid Wallace Tree Multiplier Using 4:2 Compressor in Carry Save Addition Mode

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ABSTRACT

The multiplier is one of the important elements in most of the digital processing system such as FIR filters, digital signal processors, and microprocessors etc. The speed of a system depends upon how a faster an arithmetic operations are performed within the structure for which mostly multiplication should be carried out at a faster rate which thus improves the system performance. The two important parameters of a multiplier are its area and speed that are inversely proportional.

Multipliers are of great significance in today's Digital Signal processing applications like DFT, IDFT, FFT, IFFT, and ALU in Microprocessor. Wallace tree multiplier along with a Ripple Carry adder is hybridized and formed a hybridized multiplier which delivers high speed computation along with a reduction in power consumption. Here, Wallace tree multiplier is used to increase the speed of addition and a Ripple Carry Adder is used for final accumulation. This hybrid multiplier produces better results in terms of speed and power than the conventional designs.

The proposed circuit is designed and the results are discussed in the paper. This proposed work is evaluated in the basis area, power, and delay.

***Keywords**: Hybrid Multiplier, Wallace Tree Structure, Ripple Carry Adder, Carry save Adder, 4:2 Compressor.*

1. INTRODUCTION

Many application systems based on DSP require extremely fast processing of a huge amount of digital data. The multiplier is an essential element of the digital signal processing such as filtering and convolution. Multipliers are among the fundamental components of many digital systems and, hence, their power dissipation and speed are of prime importance. In most of the portable applications, one of the most important parameters is battery power, one should reduce the power dissipation as much as possible. In every Electronic circuit, there are two major types of power dissipation i.e. static and dynamic. Out of these two, reduction in dynamic power dissipation is of prime importance. The dynamic power dissipation can be reduced by minimizing total switching activity i.e., the total number of signal transitions of the system. Continuous advances in microelectronic technologies make better use of energy, encode data more effectively and transmit information more reliably. Out of these technologies, many of them have very low power consumption for portable Electronics equipment. In these application systems, a multiplier is a fundamental arithmetic unit and widely used in circuits.

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2. SYSTEM ARCHITECTURE

Any multiplier can be divided into three stages:

1. Partial products generation stage
2. Partial products addition stage
3. Final addition stage

A lot of high-speed algorithms such as Booth's algorithm, modified Booth's algorithm, Baugh – Wooley algorithm and Braun algorithm etc. have been proposed to increase the speed of multiplier. Out of these algorithms, the Modified Booth's algorithm is the fastest algorithm because it reduces the number of partial products generation to least but at the cost of complexity and power. The speed of a multiplier is inversely proportional to the number of partial products. So, its speed can be increased by reducing by decreasing the number of partial product stages.

While designing any VLSI circuit the two important parameters to be considered are:
(I) Reduced chip area and
(II) Increased speed.

Here in our project, we are using Wallace multiplier to increase the speed and the Carry Save Adder structures to reduce the chip area. The figure below describes the Wallace multiplier where the multiplier and multiplicand are given to the encoder which thus produces the partial products followed by the Wallace tree structure which reduces the number of branches in the Wallace tree. After the reduction carried out by Wallace tree the final stage arrives giving the final products for the multiplier.

3. METHODOLOGY

A) Wallace Multiplier

A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Wallace tree is known for their optimal computation time when adding multiple operands to two outputs using 3:2 or 4:2 compressors or both. Wallace tree guarantees the lowest overall delay Fig2 shows nine operands Wallace structure, where 3:2 compressors compress the data having three multi-bit inputs and two multi-bit outputs. Using both compressors, No. of levels has been reduced that also causes enhancing the speed of multiplier.

The Wallace tree has three steps:

1. Multiply (that is AND) each bit of one of the arguments, by each bit of the other. Now, depending upon the position of the resultant multiplied bits different wires carries different weights,

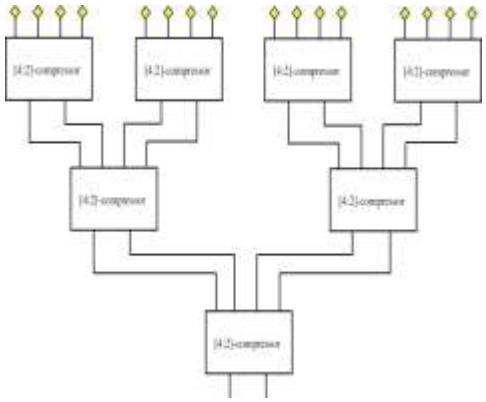

Fig1: Hybrid Wallace Tree Structure

2. Reduce the number of partial products to two by layers of full and half adders.

3. Group the wires in two numbers, and add them with a conventional adder.

B) Compressor

The 4: 2 compressors were initially designed by an intricate connection of two 3: 2 compressors as shown in Fig. 1a. The structure has a delay of four XORs. The advantage of the structure lies in its carry free nature, whereby the carry from the previous stage is not propagated to the next stage. A novel design of a 4: 2 compressor with XORs and multiplexers (MUX) as building blocks is presented in [5]. This design is based on a modified set of equations for the sum and carries outputs as:

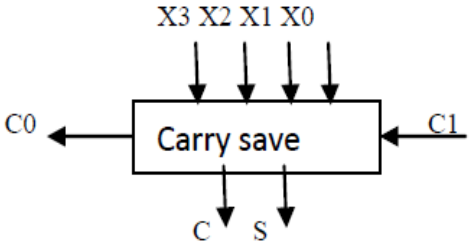

Fig2: 4:2 COMPRESSORS

$$\text{Sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_i$$

$$\text{Carry} = (x_1 \oplus x_2 \oplus x_3 \oplus x_4)c_i + \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)}x_4, \text{ and}$$

$$C_o = (x_1 \oplus x_2)x_3 + \overline{(x_1 \oplus x_2)}x_1$$

C. Unsigned Multiplier

The multiplier is one of the key hardware blocks in Digital signal processing techniques. The main aim of the multiplier is Partial Product Generation and its addition. In an n–bit

multiplier two n-bit variables are multiplied. The result of two n-bit multiplication yields a 2n-bit result. Thus, if the output is a 32-bit result then we have two 16-bit numbers as its input. The figure below shows a 32 bit unsigned multiplier.

D. Ripple Carry Adders

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using

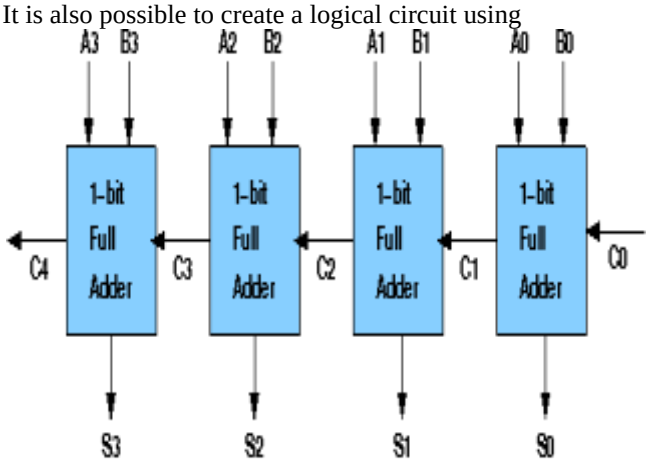

Fig: 3. Ripple Carry adder

Multiple full adders to add N-bit binary numbers. Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is "ripples" to the next full adder.

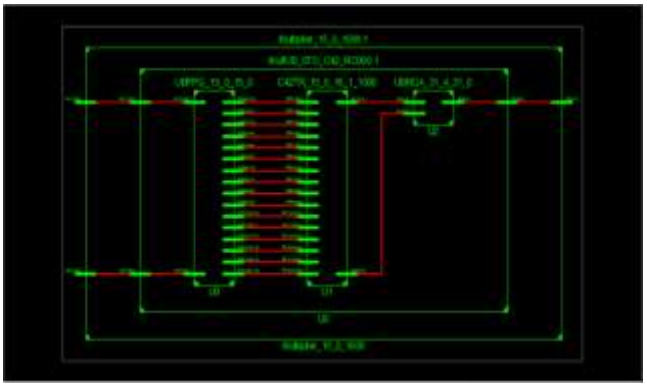

Fig 4: Hybrid Multiplier Internal Structure

Fig 5: Simulation Result of Hybrid Wallace

4. RESULT

The hybrid multiplier consisting of partial product generator, Wallace tree structure which is design by 4:2compressor.The Ripple carry adder is used for the final accumulation stage.

Table 1: Comparison Table of Multipliers

	Multiplier	Delay
1	Wallace Tree	21ns
2	Modified Wallace Tree	27ns
3	Hybrid Multiplier	8ns

5. CONCLUSION

In this paper where we have been discussing various methodology which can be adopted for designing an efficient multiplier with the help of Wallace tree and compressor. Tree based multiplier logics are the most efficient when a fewer number of bits of data are considered. The Wallace tree multiplier technique is more efficient than array multiplier. Combinational Path delay of Hybrid multiplier is 8.811 ns.

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