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Power factor correction converter using ZVS switching

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ABSTRACT

This paper proposes a soft switched single-phase high-power factor ac/dc converter. This circuit is a combination of buck converter and boost converter. In this proposes topology boost converter work as a power factor correction (PFC). Which improve power factor and reduces total harmonic distortion (THD).buck converter further regulates stable DC output voltage without using any active clamp circuit and snubber circuit. Active switches of this converter can achieve zero voltage switching (ZVS) switching with high power factor that satisfies the IEC 61000-3-2 standards. A design example for a 60W converter supplied is simulated and designed.

Keywords: *Boost converter, Buck converter, Power-factor correction (PFC), Zero-voltage switching-on (ZVS).*

1. INTRODUCTION

In this days SMPS is used in many off-line appliances, like uninterruptible power supply, telecommunications power supply, LED driver etc.[1-2].power factor correction converter is used to meet the standards of harmonic regulation such as IEC 61000-3-2 class D and IEEE 519.

Because of the advantages like easy control and modular design buck, boost or buck-boost converter is used as a power factor correction converter [3-6]. Most of high power factor ac/dc converter operate in two stages so that, circuit efficiency is somewhat reduces and it also introduce switching losses, conduction losses and mechanical core losses.

Besides the two stage approaches, cuk and Sepic converters can also achieve high power factor and regulate the output voltage[11-14] high power factor can be acquire by operating the boost converter either at discontinuous conduction mode (DCM) or continuous conduction mode (CCM).

Due to the cost effectiveness, reduces component and high efficient single stage ac-dc converter is more preferable in place of two stage topology. Some single stage approach correct power factor using half or full bridge converters. These resonant converters can operate with ZVS, if the resonant

Circuit present inductive. i.e. switching frequency is higher than resonant frequency. The active switches usually operating in hard switching so that high voltage and current stress is generated. Also high switching losses are produces. Because of that circuit became an unstable. To solve the hard switching problem some soft switching technique like snubber circuit or active clamp circuit use additional auxiliary switch, diode and reactive component. To make active switch turns on at zero voltage. So that circuit is complex and increase the overall cost.

In this paper a new ac/dc converter using ZVS with simple control is presented and analyzed. Section (2) present circuit configuration and the circuit operation for the different operating modes. Section (3) includes detailed circuit analysis and design equations. In section (4) 60W prototype circuit is built and tested to verify the result of proposed converter. Conclusion are given in section (5)

2. CIRCUIT CONFIGURATION AND OPERATION MODES

A power factor correction ac/dc converter with a two-stage circuit topology is shown in fig 1. It consists of a boost converter and a buck converter. In which, both active switches of the converter operate at hard-switching condition, resulting in high switching losses and high current and voltage stresses.

To solve the hard switching problem, a new ac/dc converter is proposed, as shown in Fig. 2. The circuit topology is derived by alteration the positions of the semiconductor devices in Fig. 1. Here, MOSFETs *S*1 and *S*2 acts as a active switches and the

antiparallel diodes *DS*1 and *DS*2 are their intrinsic body diodes, respectively. The proposed circuit mainly consists of a low-pass filter (*Lm* and *Cm*), a diode-bridge rectifier (*D*1- *D*4), a boost converter and a buck converter. The boost converter is composed of *Lp*, *DS*1, *S*2 and *Cdc* and the buck converter is composed of *Lb*, *D5*, *DS*2, *S*1 and *Co*. Both converters operate at a high-switching frequency, *fs*. When boost converter operates at discontinuous-conduction mode (DCM), it performs the function of PFC, the average value of its inductor current is a sinusoidal function [5] in every high-switching cycle. The low pass filter is used to remove the high frequency current of the inductor current so that boost converter can wave shape the input line current to be sinusoidal and in phase with the input line voltage. In other word, high power factor and low total current harmonic distortion (THDi) can be achieved. The buck converter further regulates the output voltage of the boost converter to supply stable dc voltage to the load. It is also designed to operate at DCM for achieving ZVS.

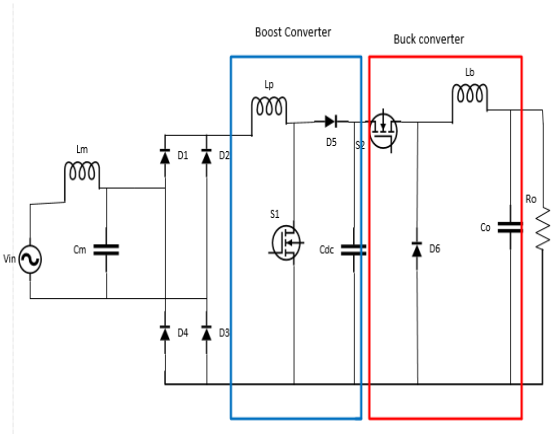


Fig. 1: Two-stage ac/dc converter

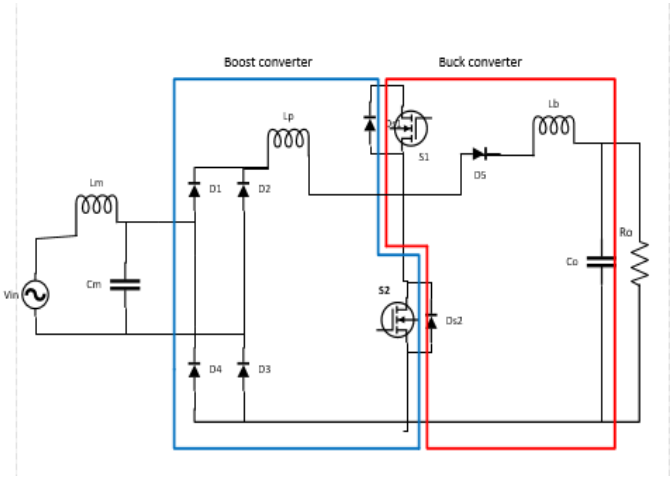


Fig. 2: Circuit topology of the proposed ac/dc converter

Two gate voltages, *vGS*1 and *vGS*2 from a half-bridge gate driver integrated circuit (IC) are used to turn *S*1 and *S*2 on and off. These voltages are complementary retectangular waveform. there is a short non-overlap time defined as "dead time" to prevent both active switches from cross conducting. In the dead time. Neglecting the short dead time, the duty cycle of *vGS*1 and *vGS*2 is 0.5.

For simplifying the circuit analysis, the following Assumptions are made:

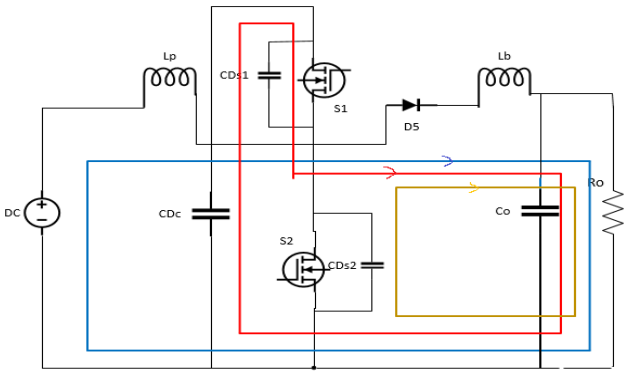
1) The semiconductor devices are ideal except for the parasitic output capacitance of the MOSFETs.
2) The capacitances of *C*dc and *C*o are large enough that the dc-link voltage *Vdc* and the output voltage *Vo* can be regarded as constant.

At steady state, the circuit operation can be divided into eight modes. Fig. 3 shows the equivalent circuits for each of the operation modes. In these equivalent circuits, the low-pass filter and the diode rectifier are represented by the rectified voltage *DC*. Fig. 4 illustrates the theoretical waveforms in each mode for the case of operating the buck converter at DCM. The circuit operation is described as follows.

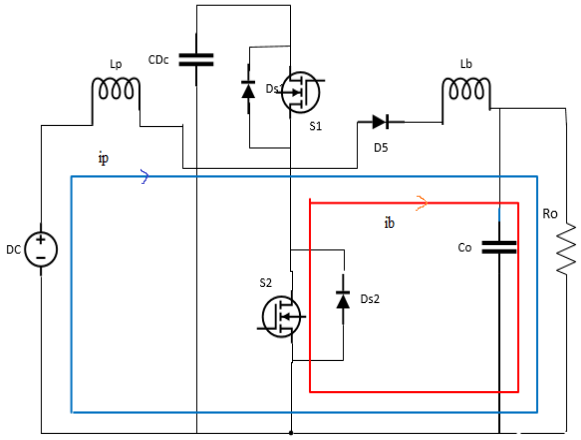
A. Mode I (t0 < t < t1)

Previous to mode I S1 is on and boost inductor current Ip is zero and DC link capacitor supplies buck inductor current ib which flows through S1, D5, Lb, Co.In mode I S1 is turned off by gate voltage Vgs1.time interval of this mode is turn off transition.ib is

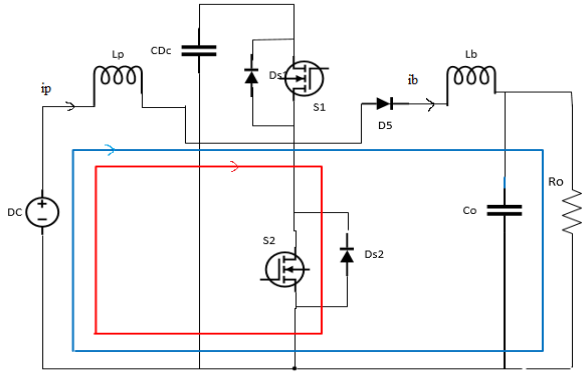
flow through output capacitance CDS1 and CDS2.in which CDS1 and CDS2 are charged and discharged respectively. When voltage across CDS2(Vds2)is lower than Vrec current ip starts to increase and when it reaches -0.7V,DS2 turns on and mode 1 ends.



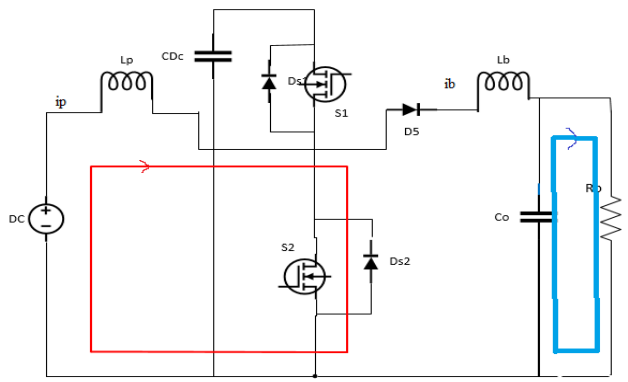
Mode I



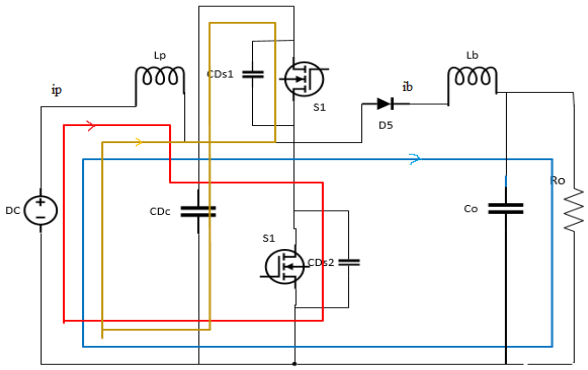
Mode II



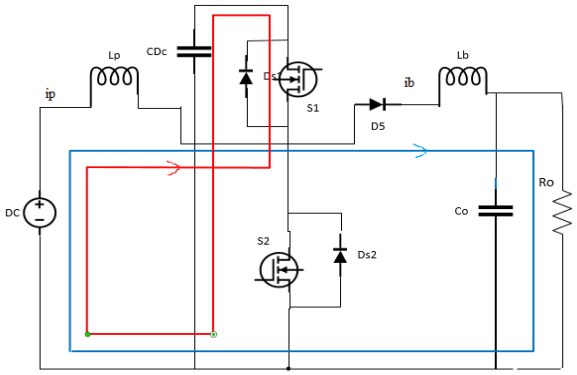
Mode III



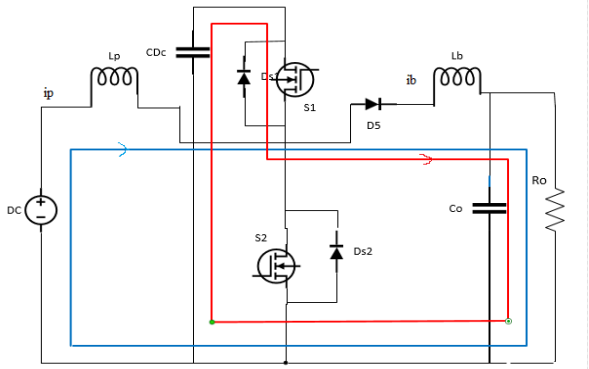
Mode IV



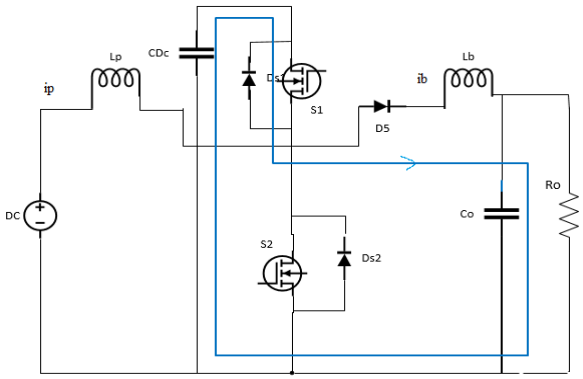
Mode V



Mode VI



Mode VII



Mode VIII

Fig. 3: Operation Modes

B. Mode II (t1 < t < t2)

At starting voltage VDS2 is maintained at about -0.7V by antiparallel diode DS2.after short dead time,S2is turn on.if the on resistance of S2 is small ib will flow through S2 from source to drain.the voltage across Lb and Lp are equal to

$vb(t) = -V0$ (1)

$vp(t) = vrec = vm|sin(2\pi fLt)|$ (2)

Where *fL*=frequency of input line voltage
Vm=amplitude of input line voltage

Mode I is very short, *ib* can be expressed as:

Ib (t) = ib (t0) - $\frac{Vo}{Lb}$ (t-t0**)** (3)

Ip (t) = $\frac{Vrec}{Lp}$ (t-t0) = $\frac{Vm|Sin(2\pi fl\,t)|}{Lp}$ (t – t0) (4)

In Mode II, *ib* is higher than *ip*. Current *ib* has two loops. This mode ends when *ip* rises to become higher than *ib*.

C. Mode III (t2 < t < t3)

In Mode III, *ip* is higher than *ib*. Current *ip* has two loops. The current direction in *S*2 is naturally changed, i.e. from drain to source. The voltage and current equations for *vb*, *vp*, *ib* and *ip* are the same as (1) – (4) Since the buck converter is designed to operate at DCM, *ib* will decrease to zero at the end of this mode.

D. Mode IV (t3 < t < t4)

In this mode, *S*2 remains on to carry *ip*. Because *ib* is zero, the buck converter is at "OFF" state and the output capacitor *Co* supplies current to load. When *S*2 is turned off by the gate voltage *vGS*2, Mode IV ends.

E. Mode V (t4 < t < t5)

When S2 off ip reaches a peak value.for maintaining flux balance ip flow through CDS1 and CDS2 when S2 is turned off.CDS1 and CDS2 is discharged and charged respectively.current ip starts increase from zero and starts to increase when voltage across CDS1 is decrease to be lower than Vdc-Vo.As Vds1 reaches -0.7V,DS1 turns on and mode V ends.

F. Mode VI (t5 < t < t6)

At the beginning of Mode VI, *vDS*1 is maintained at about -0.7 V by the antiparallel diode *DS*1. After the short dead time, *S*1 is turned on by *vGS*1. If the on-resistance of *S*1 is small enough, most of *ip* will flow through *S*1 in the direction from its source to drain. Neglecting this small value of *vDS*1, the voltage imposed on *Lp* and *Lb* can be respectively expressed as

Vp (t) = Vrec (t) – Vdc = Vm$|Sin\ (2\pi fLt)|$ – Vdc (5)
Vb (t) = Vdc – Vo (6)

ip can be expressed as:

Ip (t) = ip (t4) - $\frac{Vm|Sin(2\pi fLt) - Vdc|}{Lp}$ (t – t4) (7)

Ib (t) = $\frac{Vdc - V0}{Lb}$ (t – t4) (8)

In Mode VI, *ip* is higher than *ib*. This mode ends when *ib* rises to become higher than *ip*.

G. Mode VII (t6 < t < t7)

In Mode VII, *ib* is higher than *ip*. There are two loops for *ib*. The current direction in *S*1 is naturally changed, i.e. from drain to source. The voltage and current equations for *vp*, *vb*, *ip* and *ib* are the same as (5) – (8). Current *ib* increases continuously while *ip* keeps decreasing. The circuit operation enters next mode as soon as *ip* decreases to zero.

H. Mode VIII (t7 < t < t8)

*S*1 remains on and *ib* keeps increasing. This mode ends at the time when *vGS*1 becomes a low level to turn off *S*1 and, the circuit operation returns to Mode I of the next high frequency cycle.

From circuit operation before turning on one active switch the output capacitance is discharged about 0.7V by inductor current. then, the intrinsic body diode of active switch turns on to clamp the active voltage at nearly zero voltage. by this way each switch achieves ZVS operation.

In operation Mode II, *ip* increase and *ib* decreases and *ip* rises in proportional to the input voltage and has a small peak in nearer to zero-cross point of the input voltage. If the buck converter is operated at continuous-conduction mode (CCM), *ib* could keep higher than *ip*. On this condition, the circuit operation would not enter into Mode III and Mode IV, *CDS*1 is discharged at a high voltage of *Vdc*, resulting a spike current and high switching losses. so that buck converter is operated in DCM.

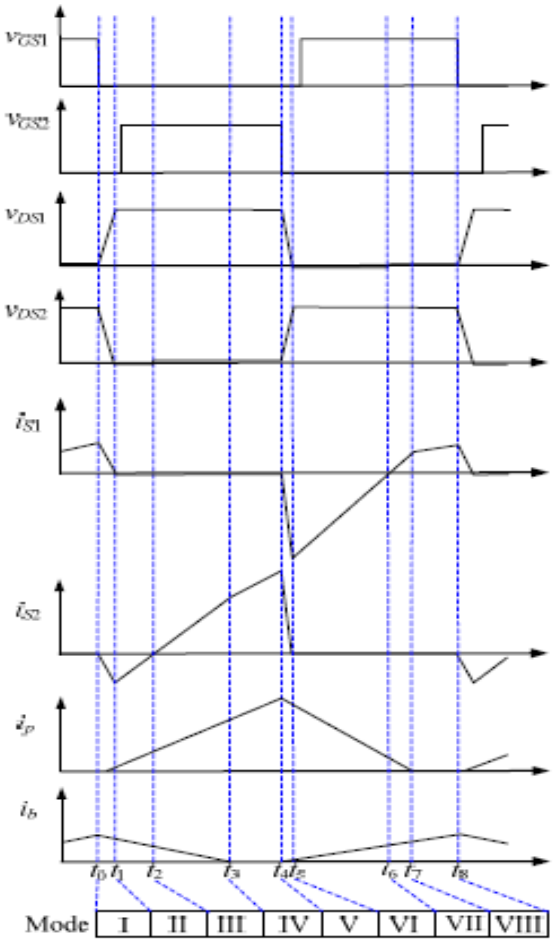


Fig. 4: Theoretical waveforms of the proposed converter

3. CIRCUIT ANALYSIS AND DESIGN

CONSIDERATION

From the circuit operation it can been seen that the antiparallel diode of one active switch of converter serves as the freewheeling diode of the other converter. The frequency of the input line voltage, *fL*, is much lower than that of the converters.

An illustrating example for driving sixty 1-W brighter LEDs is provided. These LEDs are connected in series. The rated voltage and current of each LED are 3.6 V and 0.28 A, respectively. Table I lists the circuit specifications. The input voltage is 110 Vrms ± 10%. The switching frequency is 50 kHz at rated power operation. In this design example, both converters are designed to operate at DCM. The circuit parameters are designed as follows. *Vdc* should be limited between 2*Vm* to2*Vo* [7].

DESIGN CONSIDERATION

1] Inductor Lp Design

$$Lp = \frac{\eta * Vm\hat{}\,2 * y}{8 * P0 * fs}$$

Where, η = circuit efficiency

Vm=peak input voltage

Po=output power

fs = switching frequency

From the reference [7]

$$y = \int_0^{\pi} \frac{sin^2\theta}{1-\frac{1}{k}sin\theta}\, d\theta = \frac{k^3}{\sqrt{k^2-1}}\left(1+\frac{2}{\pi}\sin^{-1}\frac{1}{k}\right) - k^2 - \frac{2}{\pi}.k$$

Where the index *k* is defined as :

$$k = \frac{Vdc}{Vm} \geq 2.3$$

2] Inductor Lb Design

$$Lb = \frac{(Vdc-V0)Vdc}{8*po*fs}$$

Where, Vdc = dc link voltage

V0 = output voltage

3] Inductance Factor AL = L/N^2

$$N = \sqrt{\frac{L}{AL}}$$

N= turns

L= inductance

For ring ferrite core R-20/10/7 AL = 2130 nH for N37

4] Output capacitance

$$C0 \geq \frac{P0}{4*fl*V0*\Delta V0}$$

Where, ΔV = ripple output voltage

5] Load resistance

$$R0 = \frac{V0}{I0}$$

6] Resonant circuit design

$$Z0 = \sqrt{\left(\frac{Lm}{Cm}\right)}$$

$$fs = 1/2\pi\sqrt{Lm * Cm}$$

Table 1: Design Specifications

Input line voltage, Vin	110V±10%,50Hz
High switching frequency,fs1,fs2	50kHz
Output power Po	60 W
Output voltage,vo	216V
Output current,Io	0.28 A

Table 2: Designed Component Values

Boost inductor Lp	0.76mH
Dc link capacitor Cdc	300nF
Output capacitance, Co	300nF
Output resistance, R_L	771ohm
Buck inductor Lb	2.14mH

Filter inductor Lm	2.16mH
Filter capacitor Cm	0.47uF

4. SIMULATION AND RESULTS

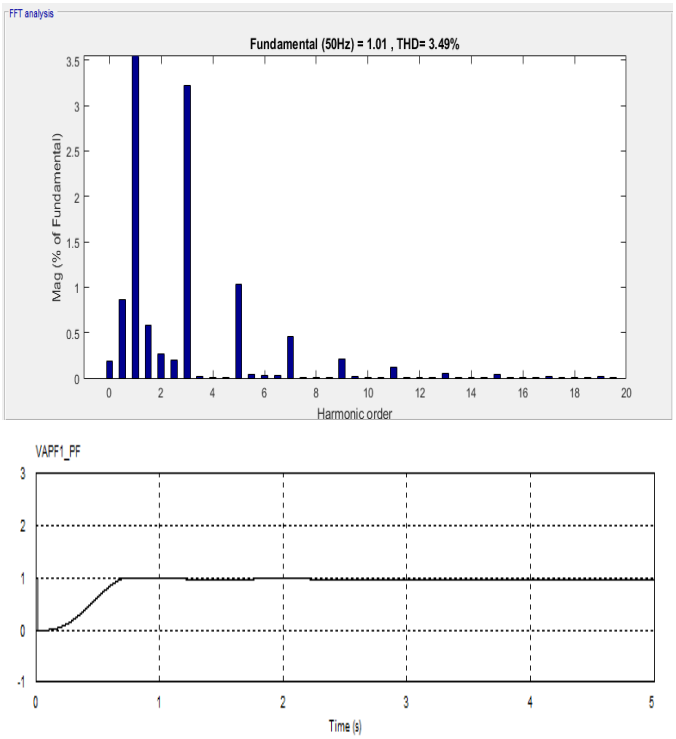
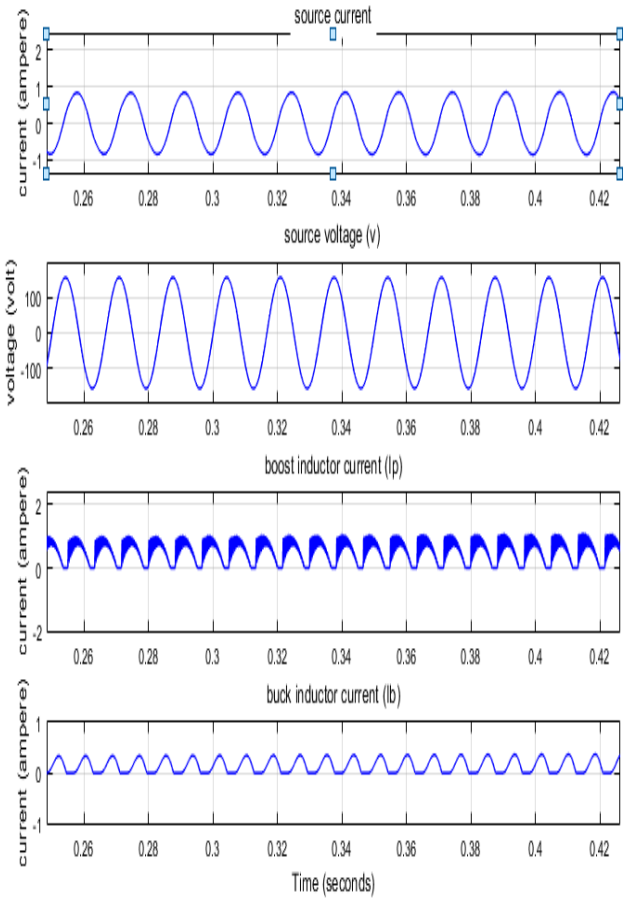


Fig 5: Harmonics and Power factor results of proposed Converter



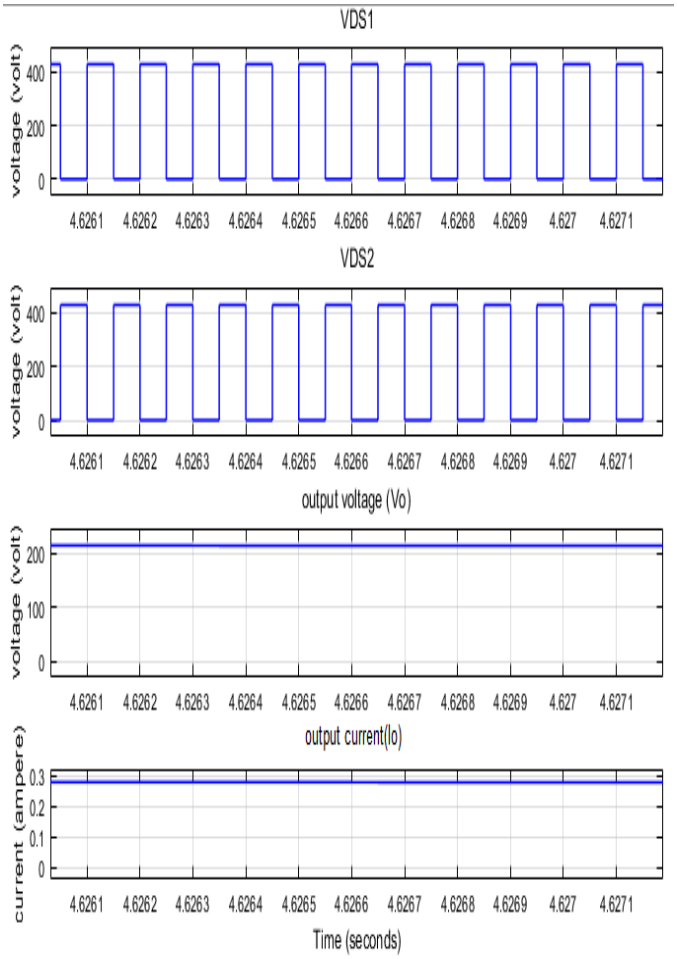


Fig 6: Simulation Results of Proposed Topology

Table 3: Simulation Results of Proposed Circuit

POWER FACTOR	**0.9983**
TOTAL HARMONIC DISTORTION	**6.67%**
EFFICIENCY	**95%**

5. CONCLUSION

A buck boost converter with ZVS provides higher circuit efficiency. The boost converter is designed to operate at DCM to perform the function of PFC. It requires that dc link voltage should be higher than two times of the amplitude of input voltage. The buck converter further regulates the dc-link voltage to obtain a stable dc voltage with low ripple. The performance parameter like low total harmonic distortion, higher power factor is achieved. Design is simple and convenient.

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