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Research Paper about SPEcint 2006

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ABSTRACT

This research paper is about CINT2006 (aka SPECint2006) and shows the relation between cores (A processor core (or simply "core") is an individual processor within a CPU), number of chips (Computer chip, also called chip, integrated circuit or small wafer of semiconductor material embedded with integrated circuitry) and a processor's performance. All these factors are taken into consideration and the performance of the processor or the result is measured. The higher the result, the better is the performance of the processor or, the less is the time taken to process the test programme instructions. Type of data : Secondary data. Independent Variables: # Cores, # Chips, # Cores Per Chip, Processor MHz Dependent Variables : Result

Keywords— *Cores, Number of Chips, Processor MHz, Result*

1. INTRODUCTION

CINT2006 (aka SPECint2006) is amongst the recent standards of SPECint, a computer benchmark specification for CPU integer processing power by the Standard Performance Evaluation Corporation (SPEC). SPECint is the integer performance testing component of the SPEC test suite. SPEC defines a base runtime for each of the 12 benchmark programs. For SPECint2006, that number ranges from 1000 to 3000 seconds. The timed test is run on the system, and the time of the test system is compared to the reference time, and a ratio is computed.

That ratio becomes the SPECint score for that test. (This differs from the rating in SPECINT2000, which multiplies the ratio by 100). As an example, for SPECint2006, consider a processor which can run 400.perlbench in 2000 seconds. The time it takes the reference machine to run the benchmark is 9770 seconds. Thus, the ratio is 4.885. Each ratio is computed, and then the geometric mean of those ratios is computed to produce an overall value. The first SPEC test suite, CPU92, was announced in 1992. It was followed by CPU95, CPU2000, and CPU2006. The dataset measures the impact of factors such as number of cores and number of chips on a processor's performance. A higher result means better performance (less time taken to process the test programme instructions).

2. OBJECTIVES

- To understand the impact of factors such as number of cores and number of chips on a processor's performance.
- To understand which processor takes less time to process the test programme instructions.

3. DATA

3.1 Cores

Class Intervals	Bin Values	Frequency
0 - 50	49	543
50 - 100	99	121
100 - 150	149	20
150 - 200	199	4
200 - 250	249	6
	More	0

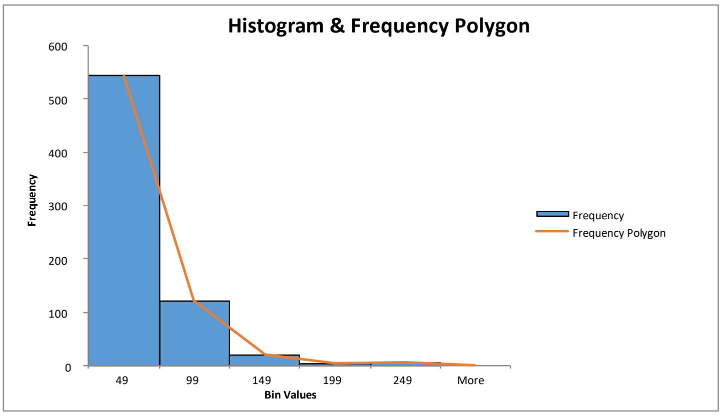


Fig. 1: Histogram and Frequency Polygon

3.2 Chips

Class Intervals	Bin Values	Frequency
0 - 2	2	552
2 - 4	4	129
4 - 6	6	0
6 - 8	8	13
	More	0

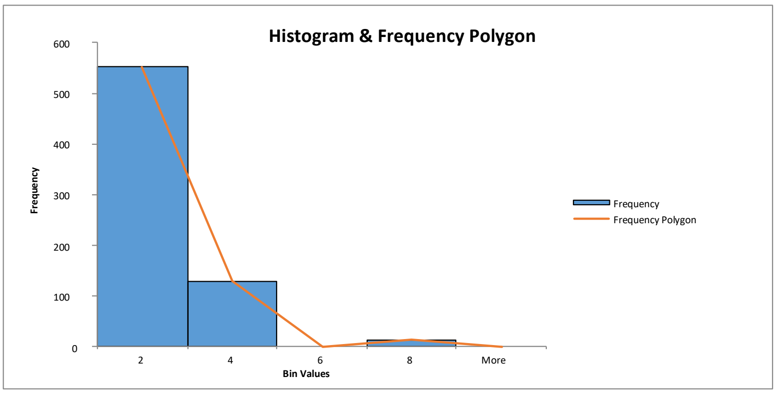


Fig. 2: Histogram and Frequency Polygon

3.3 Cores per chip

Class Intervals	Bin Values	Frequency
0 - 5	5	60
5 - 10	10	149
10 - 15	15	160
15 - 20	20	182
20 - 25	25	60
25 - 30	30	83
	More	0

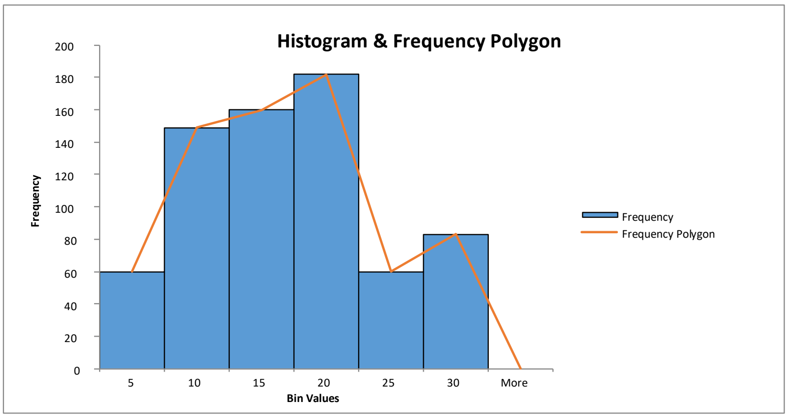


Fig. 3: Histogram and Frequency Polygon

3.4 Processor MHz

Class Intervals	Bin Values	Frequency
< 2000	1999	47
2000 - 2500	2499	378
2500 -3000	2999	139
3000 - 3500	3499	78
3500 - 4000	3999	52
	More	0

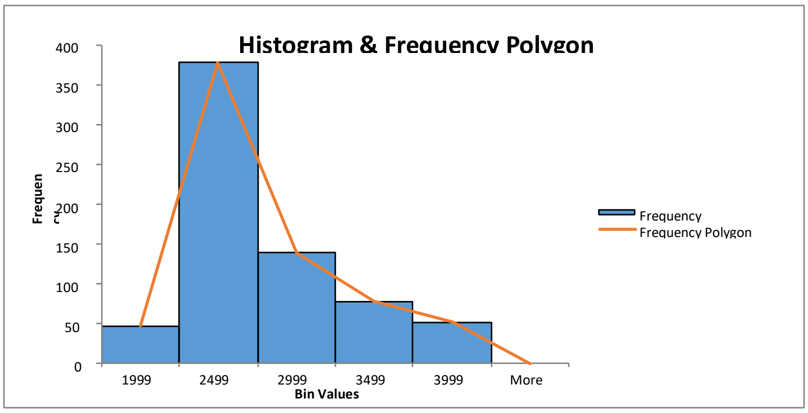


Fig. 4: Histogram and Frequency Polygon

3.5 Result

Class Intervals	Bin Values	Frequency
0 - 1000	999	148
1000 - 2000	1999	290
2000 - 3000	2999	159
3000 - 4000	3999	49
4000 - 5000	4999	29
5000 - 6000	5999	8
6000 - 7000	6999	1
7000 - 8000	7999	0
8000 - 9000	8999	3
9000 - 10000	9999	3
10000 - 11000	10999	2
11000 - 12000	11999	2
	More	0

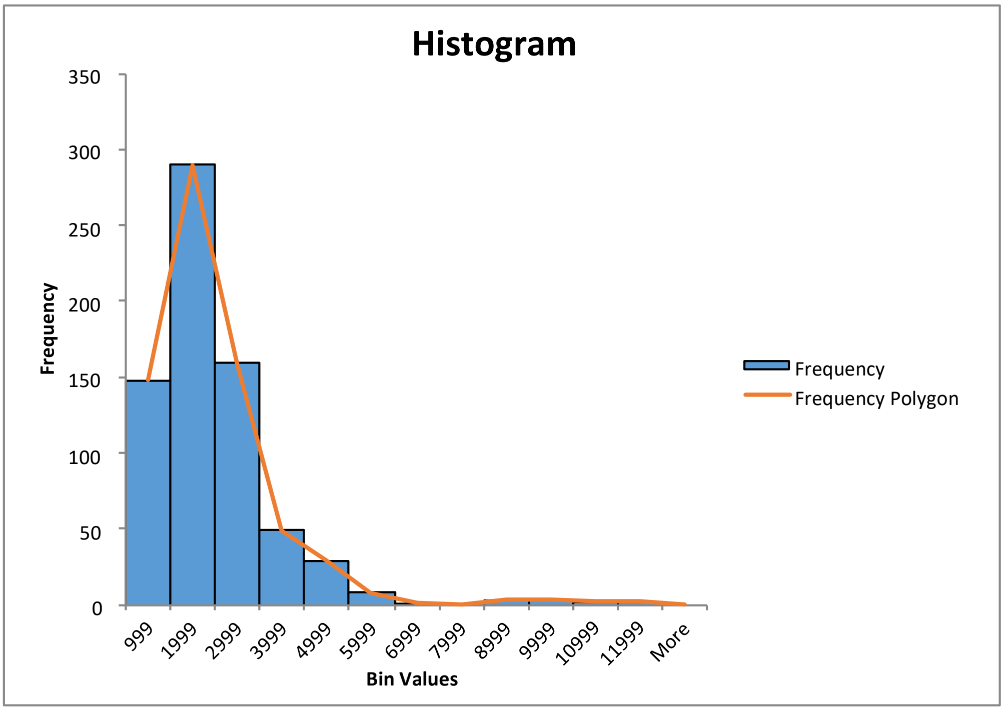
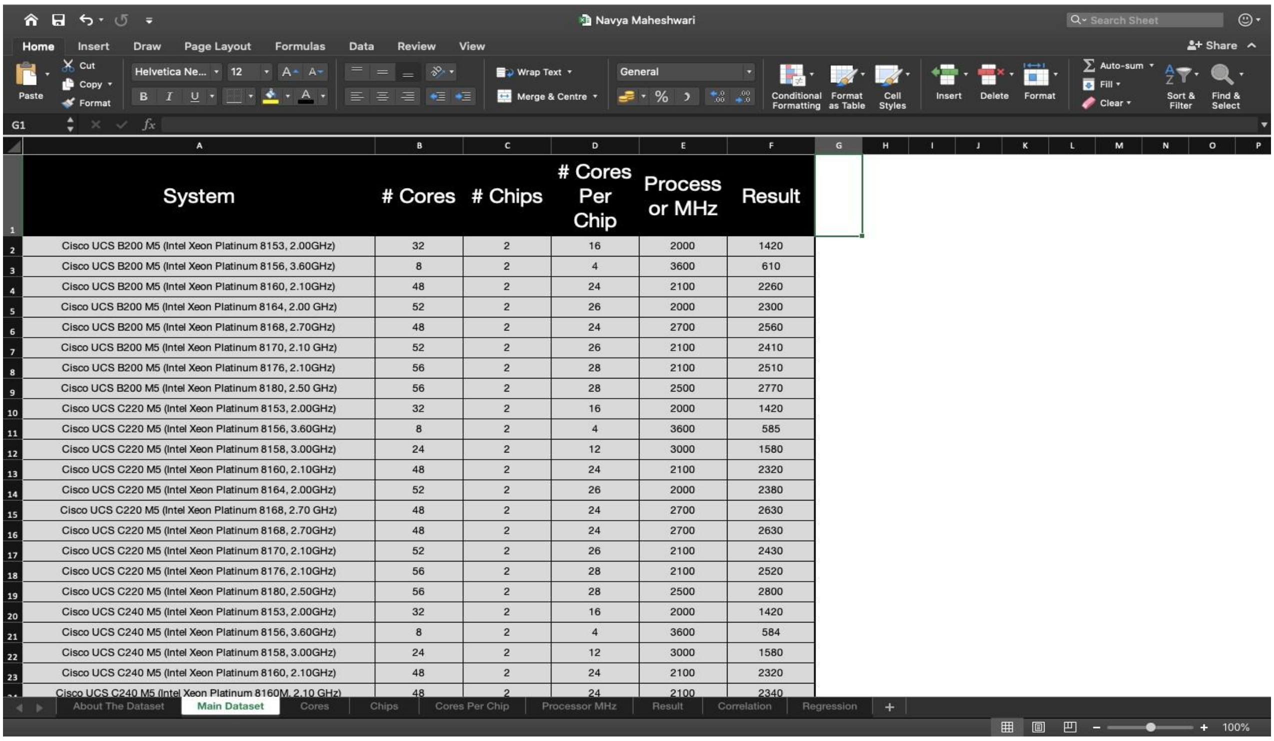


Fig. 5: Histogram



System	# Cores	# Chips	# Cores Per Chip	Process or MHz	Result
Cisco UCS B200 M5 (Intel Xeon Platinum 8153, 2.00GHz)	32	2	16	2000	1420
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60GHz)	8	2	4	3600	610
Cisco UCS B200 M5 (Intel Xeon Platinum 8160, 2.10GHz)	48	2	24	2100	2260
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)	52	2	26	2000	2300
Cisco UCS B200 M5 (Intel Xeon Platinum 8168, 2.70GHz)	48	2	24	2700	2560
Cisco UCS B200 M5 (Intel Xeon Platinum 8170, 2.10 GHz)	52	2	26	2100	2410
Cisco UCS B200 M5 (Intel Xeon Platinum 8176, 2.10GHz)	56	2	28	2100	2510
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)	56	2	28	2500	2770
Cisco UCS C220 M5 (Intel Xeon Platinum 8153, 2.00GHz)	32	2	16	2000	1420
Cisco UCS C220 M5 (Intel Xeon Platinum 8156, 3.60GHz)	8	2	4	3600	585
Cisco UCS C220 M5 (Intel Xeon Platinum 8158, 3.00GHz)	24	2	12	3000	1580
Cisco UCS C220 M5 (Intel Xeon Platinum 8160, 2.10GHz)	48	2	24	2100	2320
Cisco UCS C220 M5 (Intel Xeon Platinum 8164, 2.00GHz)	52	2	26	2000	2380
Cisco UCS C220 M5 (Intel Xeon Platinum 8168, 2.70 GHz)	48	2	24	2700	2630
Cisco UCS C220 M5 (Intel Xeon Platinum 8168, 2.70GHz)	48	2	24	2700	2630
Cisco UCS C220 M5 (Intel Xeon Platinum 8170, 2.10GHz)	52	2	26	2100	2430
Cisco UCS C220 M5 (Intel Xeon Platinum 8176, 2.10GHz)	56	2	28	2100	2520
Cisco UCS C220 M5 (Intel Xeon Platinum 8180, 2.50GHz)	56	2	28	2500	2800
Cisco UCS C240 M5 (Intel Xeon Platinum 8153, 2.00GHz)	32	2	16	2000	1420
Cisco UCS C240 M5 (Intel Xeon Platinum 8156, 3.60GHz)	8	2	4	3600	584
Cisco UCS C240 M5 (Intel Xeon Platinum 8158, 3.00GHz)	24	2	12	3000	1580
Cisco UCS C240 M5 (Intel Xeon Platinum 8160, 2.10GHz)	48	2	24	2100	2320
Cisco UCS C240 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)	48	2	24	2100	2340

4. CORRELATION

	# Cores	# Chips	# Cores Per Chip	Processor MHz	Result
# Cores	1				
# Chips	0.780016374	1			
# Cores Per Chip	0.691460583	0.175011061	1		
Processor MHz	-0.224565034	0.069212376	-0.395165334	1	
Result	0.984052357	0.812635918	0.654960348	-0.09418655	1
Interpretations					
There's an imperfect (almost pefect) positive correlation between the # Core and the result.					
There's an imperfect positive correlation between the # Chips and the result.					
There's an imperfect positive correlation between the # Core Per Chip and the result.					
There's an imperfect (very weak) negative correlation between Processor MHz and the result.					

5. REGRESSION

SUMMARY OUTPUT	
Regression Statistics	
Multiple R	0.993747385
R Square	0.987533865
Adjusted R Square	0.987461493
Standard Error	160.7612458
Observations	694

ANOVA

	df	SS	MS	F	Significance F
Regression	4	1410594311	352648577.8	13645.18446	0
Residual	689	17806638.74	25844.17814		
Total	693	1428400950			

	Coefficients	Standard Error	t Stat	P-value	Lower 95%	Upper 95%	Lower 95.0%	Upper 95.0%
Intercept	210.1255	9.6139117	4.390852	334903E-9	307.5381	9112.7129	9307.5381	9112.71299
# Cores	.973934	.7542403	2.998936	18548E-24	8.493048	1.4548198	8.4930482	1.45481928
# Chips	9.28762	5.529022	0.9013705	1.2253E-24	38.79774	99.777512	38.797742	99.7775122
# Cores Per Chip	.308664	05120711	9008357	606872E-2	6.281298	4.3360310	6.2812985	4.33603150
Processor MHz	3619767	0137661	6.2947790	86273E-10	3349481	83890052	93349481	838900529
Regression Equation								
Y = -1210.13 + 39.97X1 + 169.29X2 + 20.31X3 + 0.36X4								

Interpretations
A increase of 40.0 in # Cores will result in an increment of 1 in the result.
A increase of 169.3 in # Chips will result in an increment of 1 in the result.
A increase of 20.31 in # Cores Per Chip will result in an increment of 1 in the result.
A increase of 0.362 in Processor MHz will result in an increment of 1 in the result.

6. CONCLUSION

To conclude, a relationship between cores, number of chips and the time taken by the processor to test programme instructions was established. Using simple tools of moving averages, graphical representations and interpretations were established.

7. REFERENCES

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[2] https://en.m.wikipedia.org/wiki/SPECint, https:// www.spec.org/cpu2006/results/

